204, No. 6, p. 2010, 2007). A device formed on a double channel epitaxial structure (AlGaN/GaN/AlGaN/GaN) is discussed, where a gate trench is etched through the upper AlGaN layer stopping inside the underlying GaN layer. After etching the gate trench, a dielectric layer and a gate metal are deposited. A GaN/AlGaN/GaN structure is therefore provided under the gate, where the thickness and Al composition of the AlGaN layer is such that substantially no electrons are accumulated at the lower AlGaN/GaN interface at zero bias. The threshold voltage is typically not sensitive to the gate trench etch depth, but transport properties in the on-resistance state may be. If the GaN thickness immediately under the gate dielectric is too thick, then electrons may accumulate at the dielectric/GaN interface instead of the lower AlGaN/GaN interface under the gate in the device on-state. This may lead to a lower electron mobility and a higher device on-resistance.

SUMMARY OF THE INVENTION

[0013] Some embodiments of the present invention provide transistors including a Group III-nitride buffer layer and a Group III-nitride barrier layer on the Group III-nitride buffer layer. A non-conducting spacer layer is provided on the Group III-nitride barrier layer. The Group III-nitride barrier layer and the spacer layer define a trench extending through the barrier layer and exposing a portion of the buffer layer. A gate structure is provided on the spacer layer and in the trench and a gate electrode on the gate structure.

[0014] In further embodiments of the present invention, the trench may be further defined by the buffer layer. The transistor may further include a second non-conducting spacer layer on the gate electrode and the dielectric layer and a field plate on the second non-conducting spacer. The field plate may be electrically coupled to a source electrode or the gate electrode. The second non-conducting spacer may have a thickness of from about 500 Å to about 5000 Å.

[0015] In still further embodiments of the present invention, the trench may be further defined by the buffer layer. The transistor may further include a thin GaN layer having a thickness of from about 2.0 to about 50.0 Å between the trench and the gate structure.

[0016] In some embodiments of the present invention, the gate structure may include a dielectric layer and the dielectric layer has a thickness of from about 60 Å to about 600 Å.

[0017] In further embodiments of the present invention, the trench may be further defined by the buffer layer and the gate structure may include an aluminum nitride (AlN) layer on the spacer layer and in the trench and a dielectric layer on the AlN layer. The AlN layer may have a thickness of from about 1.0 Å to about 10.0 Å. In certain embodiments, the AlN layer may be an Aluminum Gallium Nitride (AlGaN) layer. A thin gallium nitride (GaN) layer having a thickness of from about 2.0 to about 50.0 Å may be provided between the AlN layer and the trench.

[0018] In still further embodiments of the present invention, the gate structure may include a gallium nitride (GaN) layer on the AlN layer, the GaN layer may be between the dielectric layer and the AlN layer. The GaN layer may have a thickness of from about 2.0 Å to about 30 Å. A thin gallium nitride (GaN) layer having a thickness of from about 2.0 to about 50.0 Å may be provided between the AlN layer and the trench.

[0019] In some embodiments of the present invention, the first non-conducting spacer may include silicon nitride and may have a thickness of from about 300 Å to about 3000 Å.

[0020] In further embodiments of the present invention, the gate electrode may have a length of from about 0.5 μm to about 5.0 μm.

[0021] In still further embodiments of the present invention, the transistor may be a normally-off High Electron Mobility Transistor (HEMT).

[0022] Some embodiments of the present invention provide transistors including a Group III-nitride barrier layer and a non-conducting spacer layer on the Group III-nitride barrier layer. The spacer layer defines a trench extending through the spacer layer and exposes a portion of the barrier layer. A gate implant region is provided in a portion of the barrier layer. A gate electrode is provided in the trench on the implanted region and on the spacer layer.

[0023] In further embodiments of the present invention, dielectric sidewall spacers may be provided on a sidewall of the trench. The implant region may have an implant dose of from about 5.0×10^{12} cm^{-2} to about 1.0×10^{14} cm^{-2}. The dielectric sidewall spacers may have a thickness of from about 1.0 nm to about 50.0 nm.

[0024] In still further embodiments of the present invention, the transistor may further include a second non-conducting spacer layer on the gate electrode and the spacer layer and a field plate on the second non-conducting spacer. The field plate may be electrically coupled to a source electrode or the gate electrode. The second non-conducting spacer may have a thickness of from about 500 Å to about 5000 Å.

[0025] In some embodiments of the present invention, the trench may extend into the barrier layer. The trench may extend from about 0 Å to about 200 Å into the barrier layer.

[0026] Although some embodiments of the present invention are primarily discussed above with respect to transistor embodiments, corresponding methods are also provided herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIGS. **1**A-**1**D are cross sections illustrating processing steps in the fabrication of semiconductor devices according to some embodiments of the present invention.

[0028] FIGS. **2** through **4** are cross sections illustrating semiconductor devices according to some embodiments of the invention.

[0029] FIGS. **5**A and **5**B are cross sections illustrating semiconductor devices according to some embodiments of the present invention.

[0030] FIGS. **6**A through **6**C are various graphs illustrating performance characteristics in accordance with some embodiments of the present invention.

[0031] FIGS. **7**A through **7**E are cross sections illustrating processing steps in the fabrication of semiconductor devices according to some embodiments of the present invention.

[0032] FIGS. **8** through **9**B are cross sections illustrating semiconductor devices according to some embodiments of the invention.

[0033] FIG. **10** is a graph illustrating performance characteristics in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0034] Embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are